38. (New) A MIS transistor according to claim 36, wherein said first insulator has SiN film.

B'

39. (New) A MIS transistor according to claim 38, wherein said first insulator has a larger dielectric constant than that of SiO2.

REMARKS

By this Amendment, Applicants cancel claims 10-13 and add new claims 14-39. New claim 14 corresponds to canceled claim 11, new claim 22 corresponds to canceled claim 12, new claim 32 corresponds to canceled claim 13, and new claim 34 corresponds to canceled claim 10. No new matter has been added.

In the last Office Action, the Examiner: acknowledged receipt of Applicants' Information Disclosure Statement ("IDS") filed on June 13, 2001; rejected claims 10-13 under 35 U.S.C. §112, second paragraph; rejected claim 10 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,270,257 to Shin; and rejected claims 11-13 under 35 U.S.C. § 103(a) as unpatentable over Shin and further in view of U.S. Patent No. 6,025,635 to Kirvokapic.

Regarding the acknowledgment of Applicant's IDS, a copy of the initialed PTO 1449 was not mailed to the Applicants along with the Office Action. Accordingly, Applicants respectfully request another copy from the Examiner.

The § 112 rejection of claims 10-13 is moot in view of the cancellation of these claims. Further, Applicants believe new claims 14-39 satisfy the requirements of § 112, second paragraph.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

The § 103 rejection of claim 10 is moot in view of its cancellation. Further, Applicants traverse this rejection insofar as the Examiner deems it applicable to new claim 34, which depends from independent claim 32.

Shin discloses a method of making metal oxide semiconductor field effect transistors with a lightly doped drain structure having a recess type gate. Shin discloses a polysilicon layer 24 and a thick side wall 27. The Examiner relies upon layer 24 for disclosing the claimed gate electrode. Polysilicon layer 24, however, does not have a T shape. Accordingly, Shin does not disclose or suggest a "gate electrode having a cross section of a T shape," as recited in claim 32. Thus, claim 32 is allowable over Shin. Claim 34, as well as claims 33 and 35-39, are allowable at least for their dependence from claim 32.

Claim 34 is also patentable for additional reasons. Claim 34 further recites "top surfaces of said source/drain regions have a substantially flat surface which is elevated from a top surface of said channel region and an inclined surface gradually elevated from said top surface of said channel toward said gate electrode." Nowhere does Shin disclose or suggest these features in Figs. 3C-3E. For example, Fig. 3E shows a region 26a,b which does not have a substantially flat top surface, while Fig. 3C shows a region 26a, 26b, which has a substantially flat top surface, but does not have an inclined surface gradually elevated from the top surface of the channel toward the gate electrode.

The § 103 rejection of claims 11-13 are moot in view of the cancellation of these claims. Further, Applicants traverse this rejection insofar as the Examiner deems them applicable to new claims 14, 22, and 32.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Shin teaches a thick side wall 27, which the Examiner relies upon for disclosing a gate insulator film. The Examiner admits that Shin does not teach or suggest forming a groove using the oxide as a mask, and asserts that Kirvokapic describes in Fig. 7 forming a groove using the oxide as a mask to define and form the width of each device. However, Krivokapic does not teach or suggest "forming a gate insulator film in said second groove so that a top surface of said gate insulator film is arranged farther from said semiconductor substrate than a top surface of said grooved impurity diffusion region," as recited in claims 14 and 22. Accordingly, claims 14 and 22 are patentable. Claims 15-17 and 23-26 are patentable as well, at least in view of their dependence from allowable claims 14 and 22.

A combination of Shin and Krivokapic also does not disclose "depositing a gate electrode on a top of said gate insulator film to form a gate electrode having a cross section of a T shape," as recited in claim 32. Neither Shin nor Krivokapic disclose a gate electrode having a cross section of a T shape. Shin, for example, discloses a polysilicon layer 24 that is etched back, but not in the shape of a "T". Accordingly, claim 32 is patentable.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 14, 2002

By: Tara Bleech
Tara L. Bleech
Reg. No. 46,559

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com